REMARKS

Claims 1-53 are pending.

In responding to the Examiner's prior art rejections, Applicant here only justifies the patentability of the non-allowed independent claims 1, 5, 11, 15, 22, 26, 30, 33, 37, 41, 46, and 50. As the Examiner will appreciate, should these independent claims be patentable over the prior art, narrower dependent claims would also necessarily be patentable. Accordingly, Applicant does not separately discuss the patentability of the dependent claims, although it reserves the right to do so at a later time if necessary.

The Examiner has rejected all of the independent claims 1, 5, 11, 15, 22, 26, 30, 33, 37, 41, 46, and 50 as anticipated by USP 6,449,674 ("Yun"). In this rejection, the Examiner analogizes Yun's input buffer 10 (Fig. 3) to Applicant's receiver; Yun's decoder unit 52 (Fig. 3) to Applicant's decoder; and Yun's latch unit 42 to Applicant's output timing register.

Claims 1, 5, 11, 15, 22, 30, 33, 37, 41, and 46:

As the Examiner will note, each of Applicant's rejected independent claims specify (using different language) the idea of receiving signals (e.g., at the receiver) in a first timing domain, decoding the signals (e.g., with a decoder), and outputting decoded signals (e.g., using an output timing register) in a second timing domain.

Moreover, independent claims 1, 5, 11, 15, 22, 30, 33, 37, 41, and 46 (i.e., all independent claims except claims 26 and 50 which are discussed further below) specify (using various language) that that two timing domains are established in the various circuit blocks ***in accordance with clock signals***.

This is a significant difference, and mandates that Yun cannot anticipate claims 1, 5, 11, 15, 22, 30, 33, 37, 41, and 46.

As is clear from Figure 3 of Yun, Yun's input buffers 10 receive no clock signal whatsoever. Instead, the input buffers merely "buffer each of a plurality of external control signals . . . of TTL level with a CMOS level suitable to an internal circuit operation." Col. 4, ll. 17-19. In other words, the input buffers merely change the external control signals from TTL to CMOS

signal. Otherwise, ***Yun's input buffers 10 operate in accordance with no timing domain, and instead merely buffer the control signals as they are presented to the device.***

Moreover, as the input buffers receive no clock signal, they certainly do not operate in a set timing domain ***in accordance with any clock***. But this is exactly what Applicant claims with respect to the receivers recited in independent claims 1, 5, 11, 15, 22, 30, 33, 37, 41, and 46:

> 1. . . . a receiver for receiving a plurality of signals operative in a first timing domain ***in accordance with a first clock signal***; . . . .
>
> 5. . . . a receiver for receiving a plurality of signals operative in a first timing domain ***in accordance with a first clock signal*** . . . ,
>
> 11. . . . a receiver for capturing a plurality of signals ***timed to a capture clock***;
>
> 15. . . . a FIFO synchronizer having a front end and a back end, wherein the front end is for capturing a plurality of signals operative in a first timing domain ***in accordance with a first clock signal***, ...
>
> 22. . . . a receiver for receiving a plurality of command signals operative in the sending clock domain ***in accordance with a sending clock signal***; . . . .
>
> 30. . . . means for receiving a plurality of signals operative in a first timing domain ***in accordance with a first clock signal***; . . . .
>
> 33. . . . receiving a plurality of signals operative in a first timing domain ***in accordance with a first clock signal***; . . . .
>
> 37. . . . capturing a plurality of signals ***in accordance with a capture clock of the digital circuit***; . . . .
>
> 41. . . . capturing a plurality of signals operative in a first timing domain at the front end of the FIFO synchronizer ***in accordance with a first clock signal***; . . . .
>
> 46. . . . receiving a plurality of command signals operative in the sending clock domain of the integrated circuit device ***in accordance with a sending clock signal***; . . . .

The Examiner purports to analogize Yun's "external clock" (ext_clk; Fig. 3) to the above-highlighted clock signal of Applicant claims. *See* Office Action, ¶ 3 at pg. 2. However, it is clear that ext_clk is not sent to the input to Applicant's claimed receiver, i.e., Yun's input buffers 10. Instead, that signal (after buffering; int_clk) is sent to Yun's latch units 42 (what the Examiner analogizes to Applicant's claimed output register).

In short, it is clear that Applicant's claims 1, 5, 11, 15, 22, 30, 33, 37, 41, and 46 recite limitations that are not disclosed or suggested in Yun. As a result, Yun cannot anticipate Applicant's claims.

Claim 26 and 50:

As for independent claims 26 and 50, those claims recite in different manners the concept of the receipt of an "enable signal," and decoding command signals depending on the status of the enable signal. The pertinent language from the claims is quoted below:

> 26. . . . . a receiver for receiving a plurality of command signals operative in the sending clock domain ***and for receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the circuit device is not enabled***;
> a decoder coupled to the receiver for at least partially ***decoding the command signals*** to generate at least one decoded command signal ***if the circuit device is enabled***
>
> 50. . . . . ***receiving an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the integrated circuit device is not enabled***; and
> ***if*** the enable signal indicates that the integrated circuit device is ***enabled, decoding the command signals*** to generate at least one decoded command signal . . . .

The Examiner at ¶ 7, pg. 4 of the Office Action states only the following in rejecting claims 26 and 50: "Yun teaches the receiver including a multiple-bit enabled register for each of the plurality of signals, each of the multiple-bit enabled registers being clocked using a first clock signal [buffer units 10 of Fig. 3]."

The Examiner's statements are not relevant to what is claimed. The issue recited in the claims is whether an enable signal is received to enable selective decoding of the command signals. The Examiner makes no mention of whether such an ***enable signal*** is present in Yun; instead the Examiner only states that Yun's receiver is a "multiple-bit enabled register," i.e., a register for receiving multiple bits, which is not on point to whether a signal exists in Yun that can selectively enable decoding. Indeed, such a signal is not disclosed or suggested in Yun.

Thus, as concerns claim 26, review of Figure 3 of Yun shows that Yun's input buffers 10 receive no other signal other than the command signals (e.g., /RAS, /CAS, etc.). In short, each of Yun's receivers (input buffer) do not constitute "a receiver for receiving a plurality of command

signals . . . and for receiving an enable signal" as is claimed in claim 26. Yun's receivers do not receive an enable signal, but only receive command signals.

As concerns claim 50, there simply exists no signal in Yun comprising "an enable signal with a first state in which the integrated circuit device is enabled and a second state in which the integrated circuit device is not enabled;" such that "if the enable signal indicates that the integrated circuit device is enabled, decoding the command signals" commences. Yun discloses no such signal to allow for selective decoding of the command signals, and instead they would seem to be decoded by Yun's command decoder unit 52 in all instances.

In short, claims 26 and 50 are not anticipated by Yun.

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The Applicant submits that pending claims 1-53 are patentable over the prior art of record, and requests that a Notice of Allowance issue for these claims.

Please feel free to contact the undersigned with any questions relating to this submission.

Respectfully submitted,

Nov. 1, 2005
Date

Terril G. Lewis
Registration No. 46,065

Wong, Cabello, Lutsch, Rutherford
& Brucculeri, LLP
20333 SH 249
Houston, Texas 77070
(832) 446-2422
Fax: 832 446-2424